UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,684	09/23/2003	Stefan Scholl	30169/30000	1035

4743 7590 11/02/2005

MARSHALL, GERSTEIN & BORUN LLP
233 S. WACKER DRIVE, SUITE 6300
SEARS TOWER
CHICAGO, IL 60606

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,684	SCHOLL, STEFAN	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *16-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/668,684, and Response to election/restriction filed on 08/11/2005. Applicants have elected claims 1-15 without traverse.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it does not meet requirement of a single paragraph, and includes limitation of the not elected claims, such as “manufacturing semi-conductor memory components”. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claim 1 is objected to because following informalities:

line 2, replace "a module (2)" with – a semi-conductor memory module (2) –, as recited in the claim 1 on line 6: "the semi-conductor memory module (2)".

4. Claim 12 is objected to because following informalities:

line 7, replace "an SDR" with – an SDR-DRAM --.

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-9 and 12-15 are rejected under 35 U.S.C. 102(b) as being unpatentable by Morita et al. (US Patent 6,335,901).

6. As to claim 1 Morita describes:

A process for designing semi-conductor memory components (1), in particular DRAM components, whereby the process comprises the following steps:

designing of a first layout (2') (the clock regenerating circuit 3 is deactivated thereby changing an arrangement of clock input/output circuit 2, col.13, ll.1-6, Fig.2) for a module (2) (clock input/output circuit 2, col.11, ll.57-62, Fig. 2) of the semi-conductor memory component (1) (SDRAM) to be used for a first configuration (SDRAM is

configured to operate in single data rate/SDR mode, col.13, ll.1-6) of the semi-conductor memory component (1) (col.11, ll.58-65; col.13, ll.1-15);

designing of a second layout (2") (the clock regenerating circuit 3 is activated thereby changing an arrangement of clock input/output circuit 2, col.13, ll.28-30, Fig.2) for the semi-conductor memory module (2) (clock input/output circuit 2, col.11, ll.57-62, Fig. 2) to be used for a second configuration SDRAM is configured to operate in double data rate/DDR mode, col.13, ll.28-30) of the semi-conductor memory component (1) (col.11, ll.58-65; col.13, ll.28-31);

using of the first layout (2') or of the second layout (2") for the total layout of the semi-conductor memory component (1), depending on the particular configuration of the semi-conductor memory component (1) (Abstract; col.13, ll.1-15; col.13, ll.28-31).

7. As to claims 2-9 and 12-15 Morita recites:

(2) A process according to Claim 1, in which the process comprises designing of a third layout (2"') for the semi-conductor memory component module (2) (col.13, ll.32-37);

(3), (4) A process, in which the first, second and third layouts (2', 2" 2"') for the semi-conductor memory component module (2) all have essentially the same exterior dimensions and locations (col.11, ll.58-65; col.13, ll.28-31; Fig. 2);

(5) A process according to Claim 1, in which the process additionally comprises designing of a further layout (3) (layout for a Bank 0, col.7, ll.44-45; col.7, ll.50-55; Fig. 1), not dependent on the particular configuration of the semi-conductor memory component (1), for a further module (3a) (Bank 0); (col.7, ll.22-67; col.8, ll.1-26);

(6), (7), (12) (currently amended). A process, in which the semi-conductor memory component (1) is a RAM (SDR SDRAM) or the DRAM (DDR SDRAM) component (Abstract; col.13, ll.1-15; col.13, ll.28-31);

(8) A process, in which the structure of the DRAM component (1) is essentially identical, as with DRAM components configurable by means of fuses or bonds (col.8, ll.5-18; col.37, ll.61-67; col.38, ll.1-7);

(9), (15) A process, in which additional voltage supply and address layouts to be used in RAM (SDR SDRAM) or DRAM (DDR SDRAM) components (col.13, ll.47-67; col.14, ll.1-18; col.43, ll.27-67; col.44, ll.1-22);

(13) A process, in which a number of data output bits corresponds with the particular configuration (col.37, ll.9-40);

(14) A process, in a data and/or clock pulse rate corresponds with the particular configuration (Abstract; col.13, ll.1-15; col.13, ll.28-31).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable by Morita in view of Luk et al. (US Patent 5,883,814).

With respect to claims 10-11 Morita teaches the features above but lacks a process for designing semi-conductor memory components, wherein the semi-conductor memory module (input/output structures) is allocated into different abstraction levels of the design.

9. As to claim 10-11 Luk in view of Morita teaches:

(10), (11) A process, in which the module (2) is allocated to a relatively high and/or medium semi-conductor component design abstraction level, in particular to a sub-system, algorithm, register transfer, logic and/or module level (col.5, ll.18-29; col.11, ll.52-67; col.12, ll.1-37; Fig. 14).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Luk's teaching regarding the process for designing semi-conductor memory components, wherein the semi-conductor memory module (input/output structures) is allocated into different abstraction levels of the design and use it in Morita's invention to increase an reliability of the designed semi-conductor memory components and decreasing a cost of the manufactured semi-conductor memory components.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

VUTHE SIEK
PRIMARY EXAMINER